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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/721,843 | 11/25/2003 | Steven G. Wurzer | 03-2104/L13.12-0256 | 6949 |

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|---|---|
| NGUYEN, HAI L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/721,843 | WURZER, STEVEN G. | |
| | Examiner | Art Unit | |
| | Hai L. Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-20* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claim 1 is objected to because of the following informalities: line 12, "(VCOs)" should be changed to --VCOs--. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 6, 7, and 9-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claimed limitation that "a phase-locked loop (PLL), which is fabricated on the integrated circuit and comprises a selectable loop filter capacitance and a selectable output frequency range", in claim 9, has not been enabled in the specification. Since, the specification does not enable a phase-locked loop having the claimed scope. For example, it does not enable any and every elements for performing the recited function.

Claims 6, 7, and 10-18 are rejected due to their dependencies on claim 10.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 6, 7, 9-18, and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claims 6, 7, and 9-18 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the phase/frequency detector, the charge pump, the voltage control oscillator, and the control circuit. In order for the phase locked loop (10 in instant Fig. 1) to generate a selectable output frequency range and operate as a phase locked loop, those omitted elements need to be included in the claims.

7. Claim 20 is indefinite because of the limitation "wherein (c) comprises powering down at least one current source or voltage bias generator the other VCOs in the plurality as a function of the range select signal.". It is unclear because it cannot be determined what is being claimed here.

## *Claim Rejections - 35 USC § 102*

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-4 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakanishi et al. (US 6,188,285).

With regard to claims 1 and 19, Nakanishi et al. discloses in Figs. 1-7 a phase-locked loop (PLL) circuit, and a method of use thereof, comprising a range select input (SE1, SE2), a clock output (CLK'); a phase/frequency detector (1); a charge pump (1); a loop filter (2); and a voltage-controlled oscillator (VCO) circuit coupled to the loop filter and comprising a plurality of VCOs (5, 15), which are selectively coupled between the loop filter and the clock output as a function of the range select input and have different output frequency ranges.

With regard to claim 2, each VCO has a VCO output and the PLL further comprises a multiplexer (16) having a plurality of multiplexer inputs coupled to respective VCO outputs of the plurality of VCOs, a select input controlled by the range select input and a multiplexer output coupled to the clock output.

With regard to claims 3-4, the references also meet the recited limitations in these claims.

### *Claim Rejections - 35 USC § 103*

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi et al. in view of Tobise et al. (US 6,229,399).

The above-discussed circuit of Nakanishi et al. meets all of the claimed limitations except for a control circuit (30 in instant Fig.1) and a programmable loop filter (26). Tobise et al. teaches in Figs. 4-5 a PLL circuit which comprises a control circuit (13) and a programmable

loop filter (3) having the claimed function. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to implement the control circuit and the programmable loop filter taught by Tobise et al. al. with the prior art (Figs. 1-7 of Nakanishi et al.) in order to provide more options to set the frequency range for the clock output.

### *Allowable Subject Matter*

12. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a specific structural limitations, as recited in claim 5, such as a plurality of voltage level shifters (LSH0-LSH3 in instant Figs. 3A-3B), wherein each voltage level shifter is coupled between a respective one of the VCO's (VCO0-VCO3) and the clock output (CKOUT) and is adapted to convert differential signals produced at an output of the respective VCO into a digital logic level signal (OUT, OUTN), and wherein each voltage level shifter comprises a power down input (PD, NPD in instant Figs. 5A-5B) and at least one current source or voltage bias generator (MP11, MP12, MN10, MN11, SW2), which is enabled and disabled by the power down input; and being configured in a PLL (as shown in Fig. 1) and in combination with the rest of the limitations of the base claims and any intervening claims.

***Conclusion***

13. Regarding claims 6, 7, and 9-18, the patentability thereof cannot be determined because of failing to comply with the enablement requirement and being indefiniteness.

14. Regarding claim 20, the patentability thereof cannot be determined because of its indefiniteness.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Martin et al. (US Pat. 5,686,864) is cited as of interest because it discloses a method and apparatus for controlling a voltage-controlled oscillator tuning range in a frequency synthesizer circuit.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
November 18, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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